

1 **CLAIMS**

2 1. A circuit comprising:

3 multiple components;

4 a plurality of clock drivers configured to provide separate clock signals to
5 each of the components by way of separate paths; and

6 a phase feedback element corresponding to a pair of components, wherein
7 the phase feedback element is configured to receive and adjust the phase of one of
8 the clock signals, in response to the received clock signal, to more closely match
9 the phase of the other of the clock signals.

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11 2. The circuit of claim 1, wherein the received clock signal is routed
12 along a received clock signal path which is located near the corresponding
13 components.

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15 3. The circuit of claim 1, wherein the clock signals are received at
16 adjacent ends of the components.

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18 4. The circuit of claim 1, wherein the separate paths have different
19 propagation delays.

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21 5. The circuit of claim 4, wherein the separate paths have different
22 lengths.

1 6. The circuit of claim 1, wherein the phase feedback element comprises
2 a phase comparator.

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4 7. The circuit of claim 6, wherein:
5 the phase comparator is configured to determine a phase offset; and
6 the clock drivers are responsive to the phase offsets to adjust the phases of
7 the clock signals.

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9 8. The circuit of claim 7, wherein the phase offset of the phase
10 comparator is a digital phase offset.

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12 9. The circuit of claim 1, wherein the phase feedback element comprises
13 a phase comparator that is responsive to the received component clock signals to
14 adjust the phase of the one of the received clock signals to match the phase of the
15 other of the received clock signals.

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17 10. The circuit of claim 1, wherein the phase feedback element
18 corresponding to the pair of the components comprises:

19 an integrator;
20 a first current source configured to be selectively enabled by the clock
21 signal corresponding to a first of the components of the pair of components, the
22 first current source being further configured to charge the integrator when enabled;
23 and
24 a second current source configured to be selectively enabled by the clock
25 signal corresponding to a second of the components of the pair of components, the

1 second current source being further configured to discharge the integrator when
2 enabled.

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4 11. The circuit of claim 1, wherein the phase feedback element
5 comprises:

6 a capacitive element;

7 a first current source configured to be selectively enabled by the clock
8 signal corresponding to a first of the component of the pair of components, the
9 first current source being further configured to charge the capacitive element when
10 enabled; and

11 a second current source configured to be selectively enabled by the clock
12 signal corresponding to a second of the component of the pair of components, the
13 second current source being further configured to discharge the capacitive element
14 when enabled.

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16 12. The circuit of claim 11, wherein at least one of the clock drivers is
17 responsive to a voltage at the capacitive element to adjust the phase of its clock
18 signal.

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20 13. A circuit comprising:

21 multiple components;

22 a plurality of clock drivers configured to provide separate component clock
23 signals to respectively corresponding components by way of separate paths;

24 a reference feedback element that receives a reference clock signal and a
25 clock signal from one of the components, wherein the reference feedback element

1 is configured to adjust the phase of the clock signal from one of the components,
2 in response to the reference clock signal and the received clock signal from one of
3 the components to more closely match the phase of the reference clock signal; and

4 a phase feedback element corresponding to a pair of components, wherein
5 the phase feedback element receives clock signals from each component of the
6 pair and is responsive to the received clock signals to adjust the phase of one of
7 the clock signals to match the phase of the other of the clock signals; wherein the
8 clock signals received by the reference feedback element and the phase feedback
9 element are routed from near the corresponding components.

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11 **14.** The circuit of claim 13, wherein the separate paths have different
12 propagation delays.

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14 **15.** The circuit of claim 13, wherein the separate paths have different
15 lengths.

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17 **16.** The circuit of claim 13, wherein the reference feedback element and
18 the phase feedback element comprise phase comparators.

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20 **17.** The circuit of claim 13, wherein:
21 the reference feedback element and phase feedback elements comprise
22 phase comparators;
23 each phase comparator is configured to determine a phase offset; and
24 the clock drivers are responsive to the phase offsets to adjust the phases of
25 the clock signals of the components.

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2 **18.** The circuit of claim 17, wherein the phase offset is a digital phase
3 offset.

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5 **19.** The circuit of claim 13, wherein the phase feedback element
6 comprises:

7 an integrator;
8 a first current source configured to be selectively enabled by the clock
9 signal corresponding to a first component of the pair of components, the first
10 current source being further configured to charge the integrator when enabled; and
11 a second current source configured to be selectively enabled by the clock
12 signal corresponding to a second component of the pair of components, the second
13 current source being further configured to discharge the integrator when enabled.

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15 **20.** The circuit of claim 13, wherein the phase feedback element
16 comprises:

17 a capacitive element;
18 a first current source configured to be selectively enabled by the clock
19 signal corresponding to a first component of the pair of components, the first
20 current source being further configured to charge the capacitive element when
21 enabled; and
22 a second current source configured to be selectively enabled by the clock
23 signal corresponding to a second component of the pair of components, the second
24 current source being further configured to discharge the capacitive element when
25 enabled.

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2 **21.** The circuit of claim 20, wherein at least one of the clock drivers is
3 responsive to a voltage at the capacitance to adjust the phase of its component
4 clock signal.

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6 **22.** A circuit comprising:
7 multiple components;
8 a plurality of clock drivers configured to provide separate clock signals to
9 corresponding components by way of separate paths; and
10 a phase comparator corresponding to a pair of components, wherein the
11 phase comparator receives the clock signals from each component of the pair of
12 components and is responsive to the received component clock signals to generate
13 a phase offset;
14 the clock drivers being responsive to phase offsets to synchronize the
15 component clock signals at the components.

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17 **23.** The circuit of claim 22, wherein a first component of the pair
18 components comprises a first plurality of bit registers arranged in a first sequence
19 and a second component of the pair components comprises a second plurality of
20 bit registers arranged in a second sequence and wherein the clock drivers provide
21 separate clock signals to each of the bit registers in each of the components of the
22 pair of components via separate paths.

1 **24.** The circuit of claim 23, wherein the first and second components of
2 the pair of components are located such that a first bit register of the second
3 plurality of bit registers is located adjacent a last bit register of the first plurality of
4 bit registers.

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6 **25.** The circuit of claim 24, wherein the phase comparator receives the
7 clock signals from the first bit register of the second plurality of bit registers and
8 the last bit register of the first plurality of bit registers.

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10 **26.** The circuit of claim 25, wherein the clock signals received by the
11 phase comparator from the first bit register of the second plurality of bit registers
12 and the last bit register of the first plurality of bit registers are routed on paths that
13 are length matched.

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15 **27.** The circuit of claim 22, wherein the clock signals are received at
16 adjacent ends of the components.

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18 **28.** The circuit of claim 22, wherein the component clock signals
19 received by the phase comparator are routed from near the corresponding
20 components.

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22 **29.** The circuit of claim 22, wherein the separate paths have different
23 propagation delays.

1 **30.** The circuit of claim 29, wherein the separate paths have different
2 lengths.

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4 **31.** The circuit of claim 22, wherein the phase offset is a digital phase
5 offset.

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7 **32.** The circuit of claim 22, wherein the phase offset is an analog phase
8 offset.

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10 **33.** A method of synchronous clocking, comprising:
11 routing separate clock signals to corresponding components;
12 comparing phases of clock signals received at a pair of component;
13 adjusting the clock signal received at one of the components to match the
14 phase of the clock signal received at the other one of the components.

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16 **34.** The method of claim 33, wherein the clock signals are received at
17 adjacent ends of the components.

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19 **35.** The method of claim 33, wherein the comparing comprises charging
20 and discharging a capacitive element in response to the clock signals.

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22 **36.** One or more components comprising:
23 means for routing individual clock signals to corresponding components;
24 means for comparing phases of clock signals received at a pair of
25 components;

1 means for adjusting a clock signal from one of the components to match the
2 phase of a reference clock signal; and

3 means for adjusting the clock signal received at one of the components to
4 match the phase of the clock signal received at the other one of the components.

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